# LCD DUPLEX DRIVER

## GENERAL DESCRIPTION

The PCE2111 is a single chip, silicon gate C-MOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcomputers. All inputs are C-MOS/N-MOS compatible.

### Features

- 64 LCD-segment drive capability.
- Supply voltage 2,25 to 6,5 V.
- Low current consumption.
- Serial data input.
- CBUS control.
- One-point built-in oscillator.
- Expansion possibility.



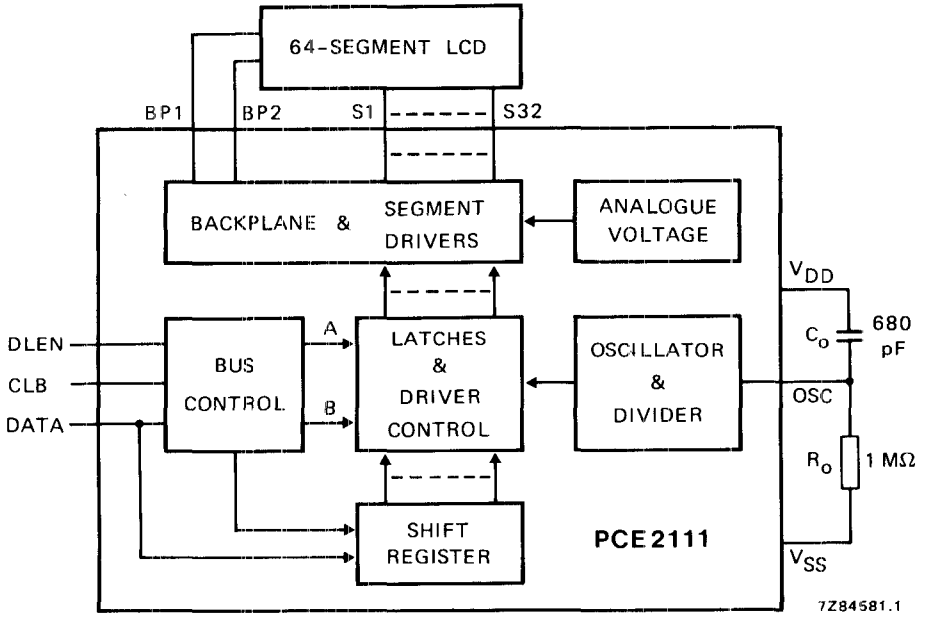


Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCE2111P: 40-lead DIL; plastic (SOT-129).
PCE2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

# LCD DUPLEX DRIVER

## GENERAL DESCRIPTION

The MH111 is a single chip, silicon gate C-MOS circuit designed to drive an LCD-display (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcomputers. All inputs are C-MOS/N-MOS compatible.

### Features

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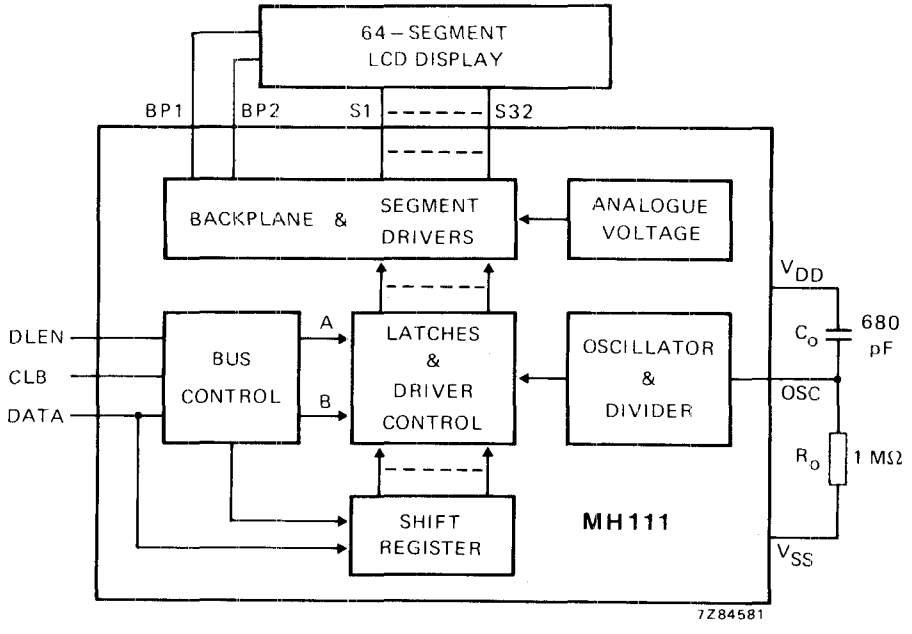


Fig. 1 Block diagram; DLEN = data line enable; CLB = clock burst; DATA = data line.

## PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129) and 40-lead flat-pack; plastic (SO-40; SOT-158).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---|---|---|
| Supply voltage with respect to $V_{SS}$ | $V_{DD}$ | −0,3 to 8 V |
| Voltage on any pin | $V_{SS}$ | −0,3 to $V_{DD}$ + 0,3 V |
| Operating ambient temperature range | $T_{amb}$ | −25 to + 85 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

## CHARACTERISTICS

$V_{DD}$ = 2,25 to 6,5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −25 to + 85 °C; $R_o$ = 1 MΩ; $C_o$ = 680 pF; unless otherwise specified

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply current | no external load | $I_{DD}$ | – | 10 | 30 | μA |
| Display frequency | see Fig. 8; T = 680 μs | $f_{LCD}$ | 60 | 80 | 100 | Hz |
| D.C. component of LCD drive | with respect to $V_{SX}$ | $V_{BP}$ | – | ± 10 | – | mV |
| Load on each segment driver | | | – | – | 10 | MΩ |
| | | | – | – | 500 | pF |
| Load on each backplane driver | | | – | – | 1 | MΩ |
| | | | – | – | 5 | nF |
| Input voltage HIGH | see Fig. 9 | $V_{IH}$ | 2 | – | – | V |
| Input voltage LOW | see Fig. 9 | $V_{IL}$ | – | – | 0,6 | V |
| Rise time $V_{BP}$ to $V_{SX}$ | max. load | $t_r$ | – | 20 | – | μs |
| **Inputs CLB, DATA, DLEN** | see note | | | | | |
| Input capacitance | for SOT-129 package | $C_{IN}$ | – | – | 10 | pF |
| | for SOT-158A package | $C_{IN}$ | – | – | 5 | pF |
| Rise and fall times | see Fig. 2 | $t_r$, $t_f$ | – | – | 10 | μs |
| CLB pulse width HIGH | see Fig. 2 | $t_{WH}$ | 1 | – | – | μs |
| CLB pulse width LOW | see Fig. 2 | $t_{WL}$ | 9 | – | – | μs |

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---|---|---|
| Supply voltage with respect to $V_{SS}$ | $V_{DD}$ | −0,3 to 8 V |
| Voltage on any pin | $V_{SS}$ | −0,3 to $V_{DD}$ + 0,3 V |
| Operating ambient temperature range | $T_{amb}$ | −25 to + 85 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## CHARACTERISTICS

$V_{DD}$ = 3 V; $V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $R_o$ = 1 MΩ; $C_o$ = 680 pF; unless otherwise specified

| *parameter* | *condition* | *symbol* | *min.* | *typ.* | *max.* | *unit* |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{DD}$ | 2,25 | 3 | 6,5 | V |
| Supply current | no external load | $I_{DD}$ | – | 10 | 50 | μA |
| Clock frequency | see Fig. 8 | $f_{CLB}$ | – | – | 125 | kHz |
| Display frequency | see Fig. 6; T = 680 μs | $f_{LCD}$ | 60 | 80 | 100 | Hz |
| D.C. component of LCD drive | with respect to $V_{SX}$ | $V_{BP}$ | – | ± 10 | – | mV |
| Load on each segment driver | | | – | – | 10 | MΩ |
| | | | – | – | 500 | pF |
| Load on each back plane driver | | | – | – | 1 | MΩ |
| | | | – | – | 5 | nF |
| Input voltage HIGH | $V_{DD}$ = 2,25 to 6,5 V with respect to $V_{SS}$; see Fig. 7 | $V_{IH}$ | 2 | – | – | V |
| Input voltage LOW | | $V_{IL}$ | – | – | 0,6 | V |
| Rise time $V_{BP}$ to $V_{SX}$ | max. load | $t_r$ | – | 20 | – | μs |

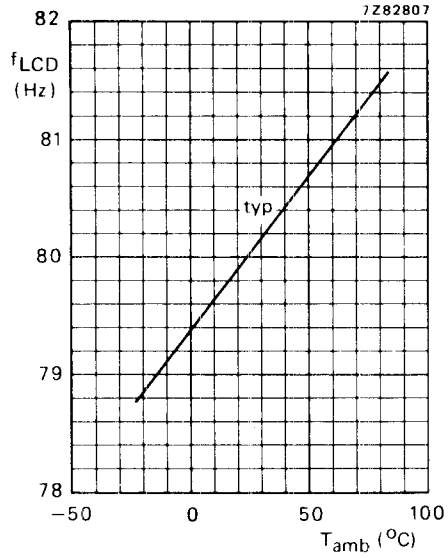


Fig. 2 Display frequency as a function of ambient temperature; $V_{DD}$ = 3 V; $R_oC_o$ = 680 μs.

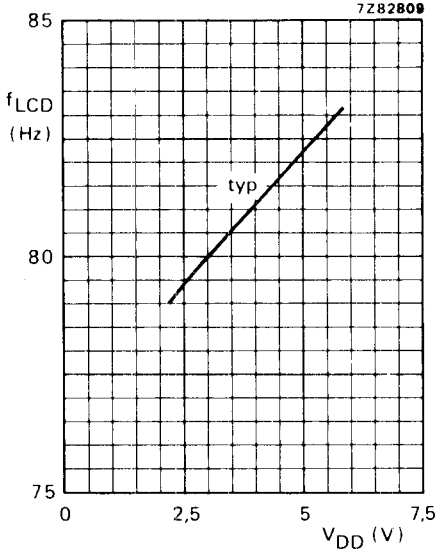


Fig. 3 Display frequency as a function of supply voltage; $T_{amb}$ = 25 °C; $R_oC_o$ = 680 μs.

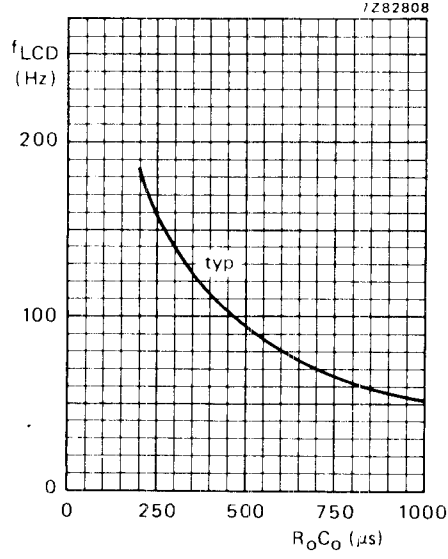


Fig. 4 Display frequency as a function of $R_o$ x $C_o$ time; $T_{amb}$ = 25 °C; $V_{DD}$ = 3 V.

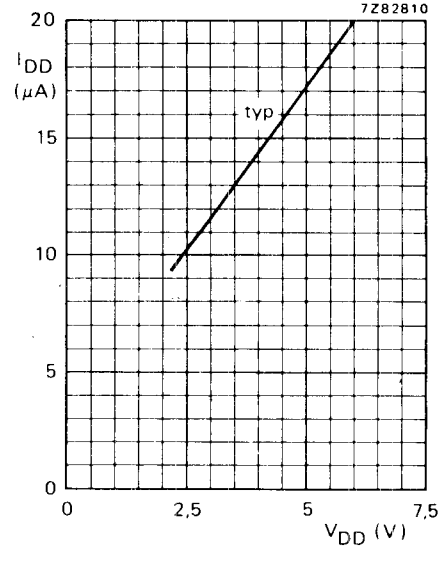


Fig. 5 Supply current as a function of supply voltage; $T_{amb}$ = 25 °C.

CHARACTERISTICS (continued)

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Data set-up time DATA → CLB | see Fig. 2 | $t_{SUDA}$ | 8 | – | – | μs |
| Data hold time DATA → CLB | see Fig. 2 | $t_{HDDA}$ | 8 | – | – | μs |
| Enable set-up time DLEN → CLB | see Fig. 2 | $t_{SUEN}$ | 1 | – | – | μs |
| Disable set-up time CLB → DLEN | see Fig. 2 | $t_{SUDI}$ | 8 | – | – | μs |
| Set-up time (load pulse) DLEN → CLB | see Fig. 2 | $t_{SULD}$ | 8 | – | – | μs |
| Busy-time from load pulse to next start of transmission | see Fig. 3 | $t_{BUSY}$ | 8 | – | – | μs |
| Set-up time (leading zero) DATA → CLB | see Fig. 2 | $t_{SULZ}$ | 8 | – | – | μs |

**Note**

All times are measured with a voltage swing of minimum $V_{IH}$ to $V_{IL}$ (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

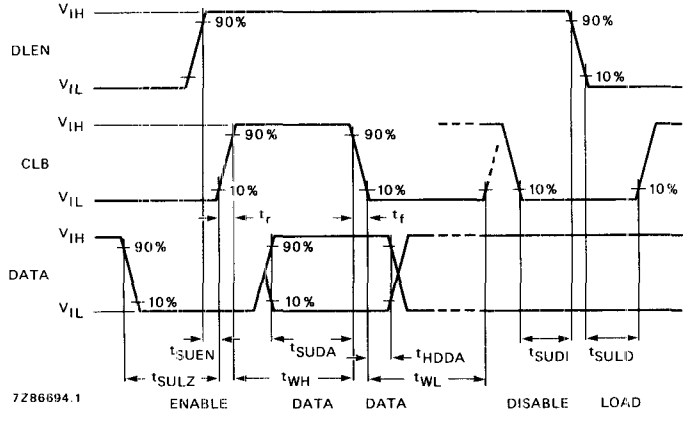


Fig. 2 CBUS timing.

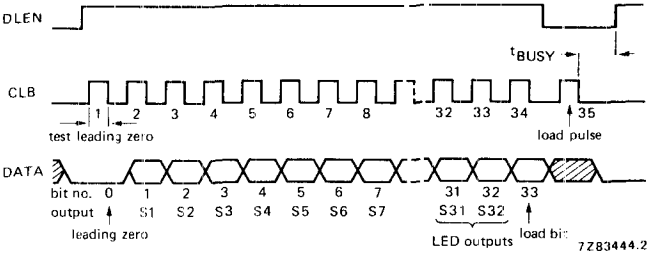


Fig. 3 CBUS data format.

**Notes to Fig. 3**

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If all test conditions are not fullfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

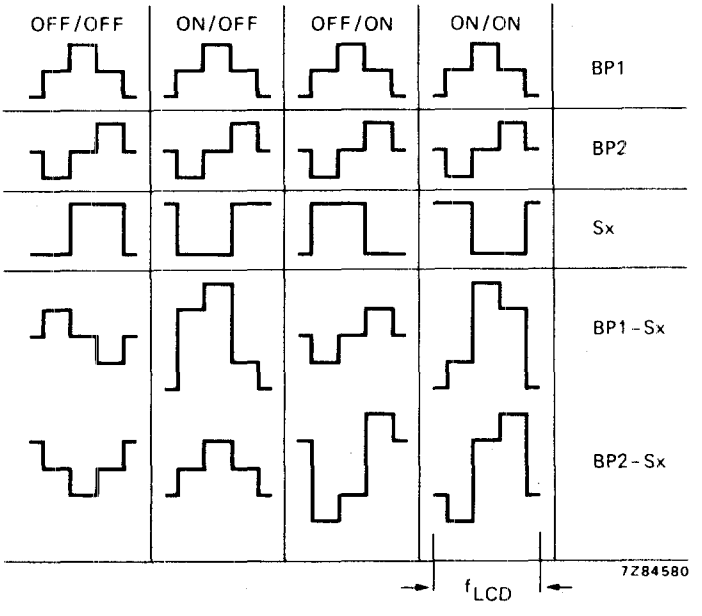


Fig. 6 Timing diagram.

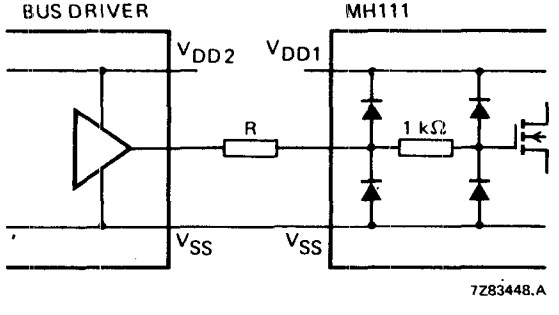


Fig. 7 Input circuitry.

Note to Fig. 7

$V_{SS}$ line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.

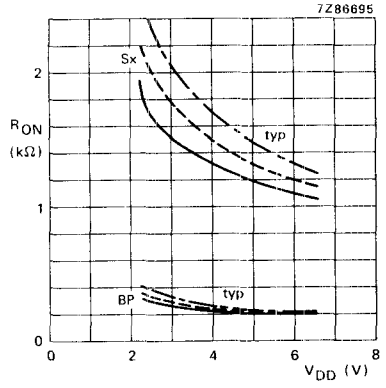


Fig. 4 Output resistance of backplane and segments.
——— $T_{amb}$ = −40 °C; − − − $T_{amb}$ = + 25 °C; − · − · $T_{amb}$ = +85 °C.

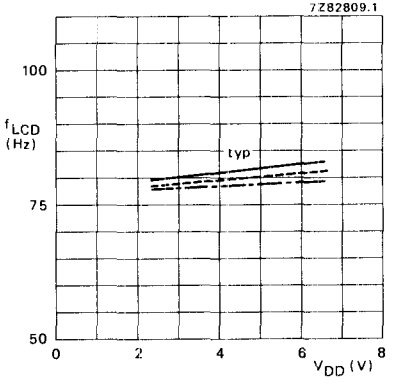


Fig. 5 Display frequency as a function of supply voltage; $R_oC_o$ = 680 μs.
——— $T_{amb}$ = −40 °C; − − − $T_{amb}$ = + 25 °C; − · − · $T_{amb}$ = +85 °C.

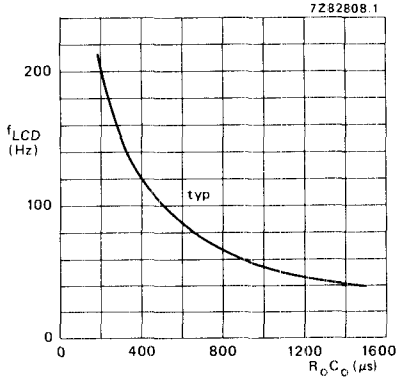


Fig. 6 Display frequency as a function of $R_o$ x $C_o$ time; $T_{amb}$ = 25 °C.

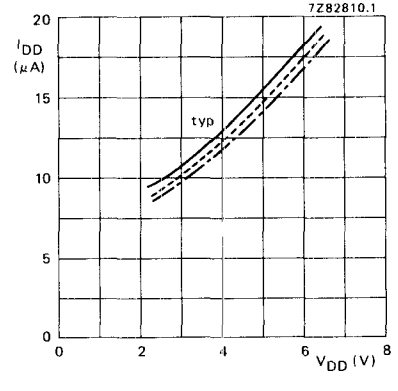


Fig. 7 Supply current as a function of supply voltage.
——— $T_{amb}$ = −40 °C; − − − $T_{amb}$ = +25 °C; − · − · $T_{amb}$ = +85 °C.

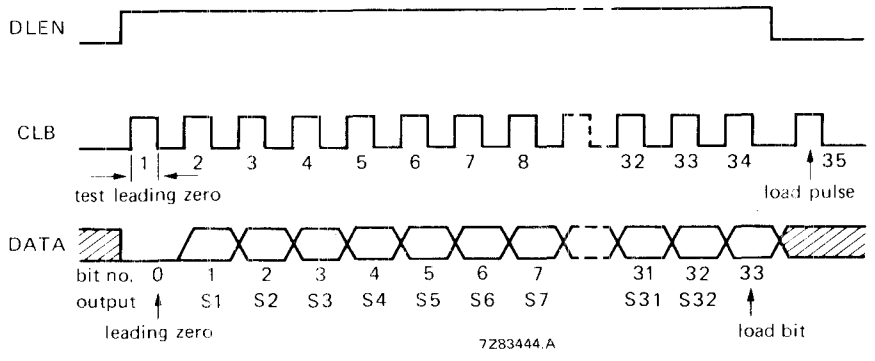


Fig. 8 Data format.



Notes to Fig. 8

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

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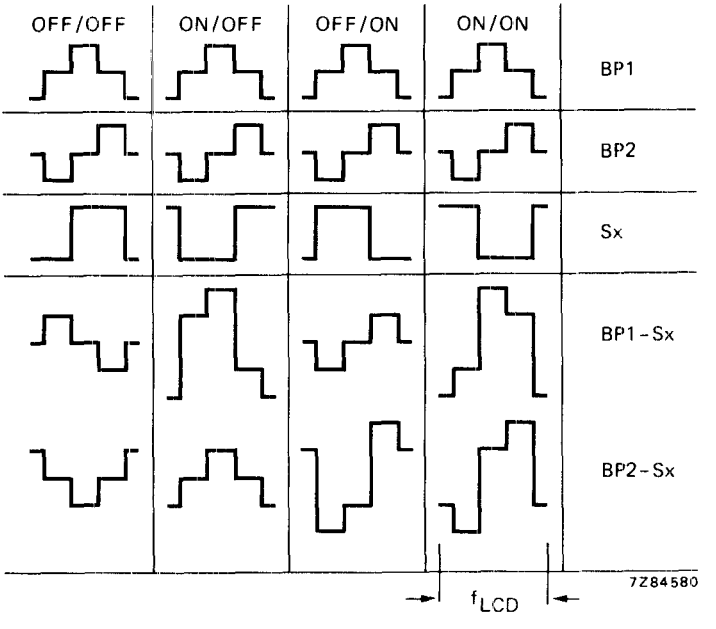



Fig. 8 Timing diagram.

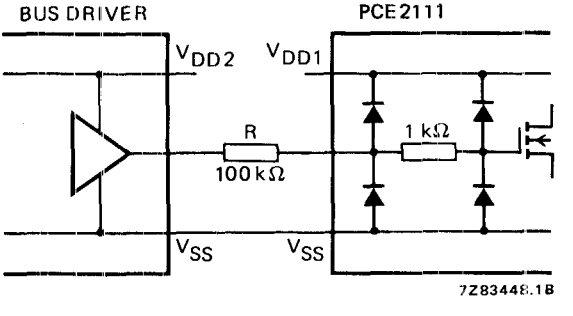



Fig. 9 Input circuitry.

**Note to Fig. 9**

$V_{SS}$ line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant$ 40 $\mu$A.

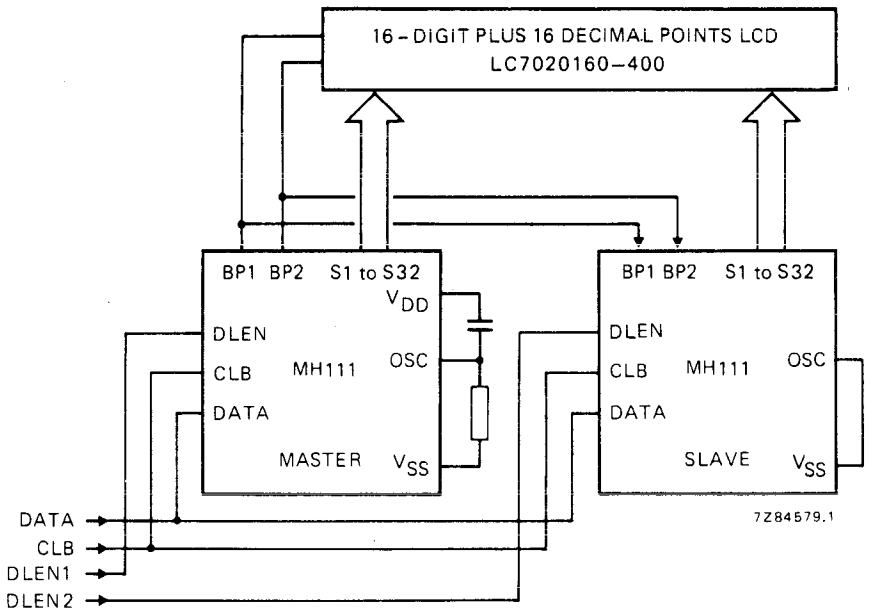



Fig. 9 Diagram showing expansion possibility for a 16-digit plus 16 decimal points LCD.

Note to Fig. 9

By connecting OSC to $V_{SS}$ the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several MH111, MH110 and MH100 ICs up to the BP drive capability of the master.

MH100 is a 40 LCD-segment display driver; MH110 is a 60 LCD-segment display driver plus 2 LED driver outputs.

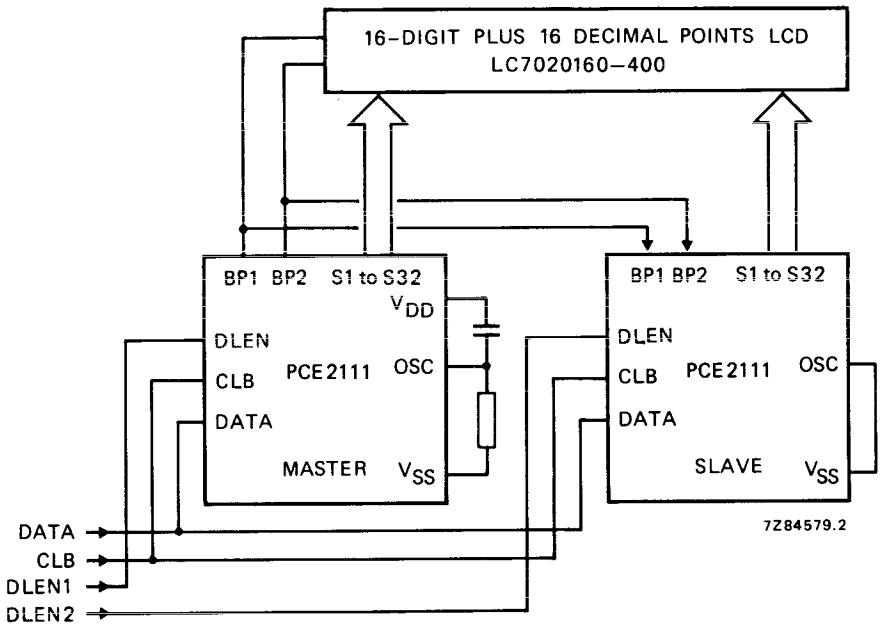



Fig. 10 Diagram showing expansion possibility for a 16-digit plus 16 decimal points LCD.

**Note to Fig. 10**

By connecting OSC to $V_{SS}$ the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCE2111, PCE2110 and PCE2100 ICs up to the BP drive capability of the master.

PCE2100 is a 40 LCD-segment driver; PCE2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

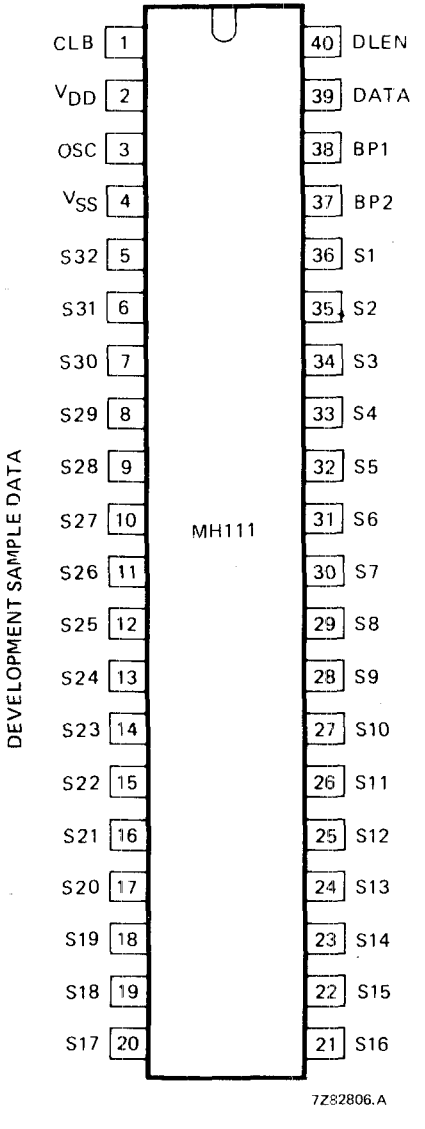



Fig. 10 Pinning diagram.

## PINNING

### Supply

| | | |
|---|---|---|
| 2 | $V_{DD}$ | Positive supply |
| 4 | $V_{SS}$ | Negative supply |

### Inputs

| | | |
|---|---|---|
| 3 | OSC | Oscillator input |
| 39 | DATA | Data line |
| 40 | DLEN | Data line enable |
| 1 | CLB | Clock burst |

### Outputs

| | | |
|---|---|---|
| 38 | BP1 | Back plane drivers (common of LCD display) |
| 37 | BP2 | |
| S1 to S32 | | LCD driver outputs |

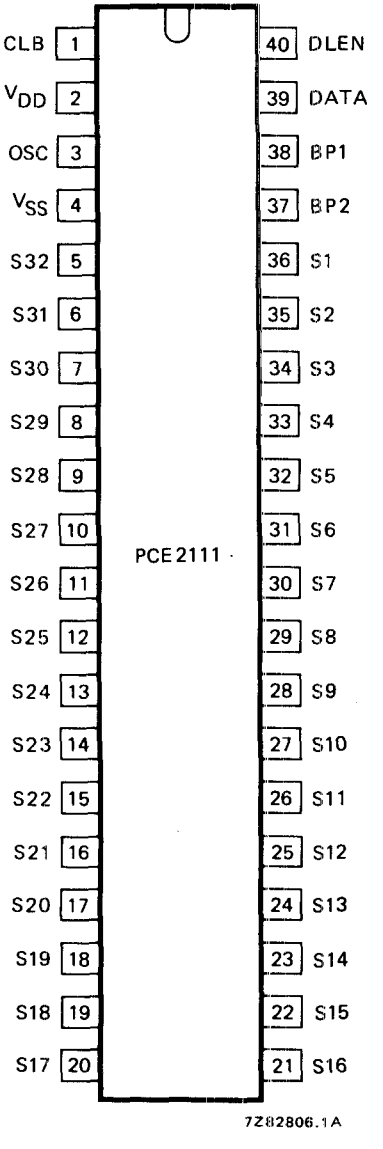



Fig. 11 Pinning diagram.

## PINNING

### Supply

| | | |
|---|---|---|
| 2 | $V_{DD}$ | Positive supply |
| 4 | $V_{SS}$ | Negative supply |

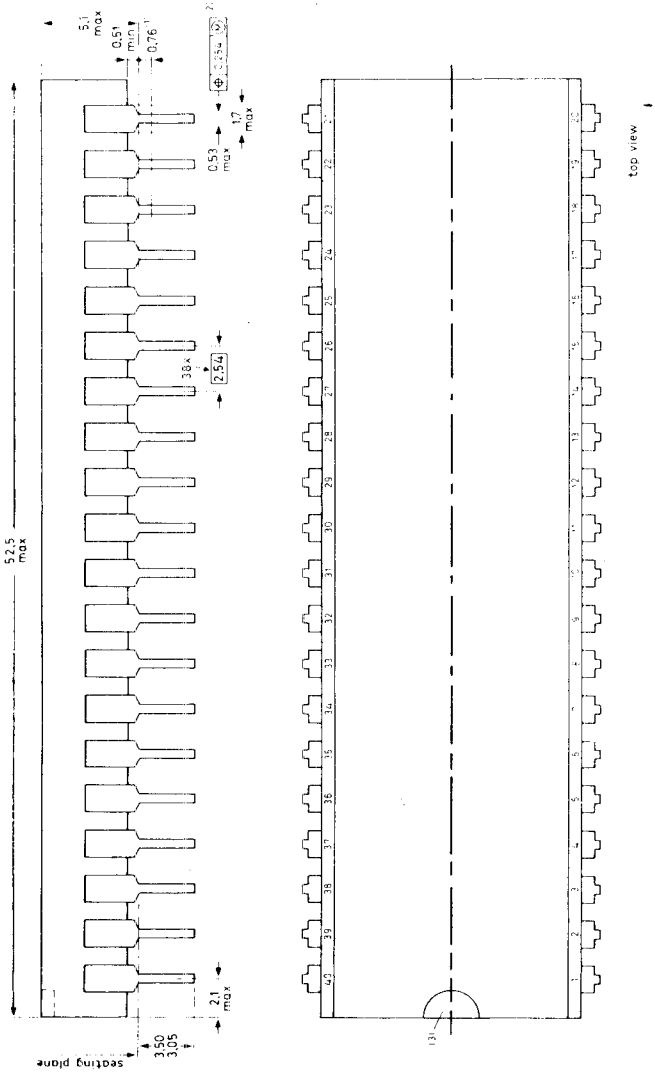
### Inputs

| | | | |
|---|---|---|---|
| 3 | OSC | Oscillator input | |
| 39 | DATA | Data line | CBUS |
| 40 | DLEN | Data line enable | CBUS |
| 1 | CLB | Clock burst | CBUS |

### Outputs

| | | |
|---|---|---|
| 38 | BP1 | Backplane drivers (common of LCD) |
| 37 | BP2 | Backplane drivers (common of LCD) |
| S1 to S32 | | LCD driver outputs |

# 40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)




Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

**SOLDERING**

See next page.

## SOLDERING

**1. By hand**

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

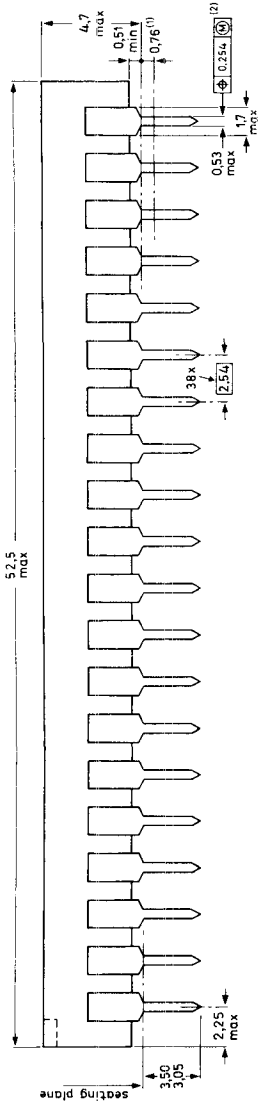
**2. By dip or wave**

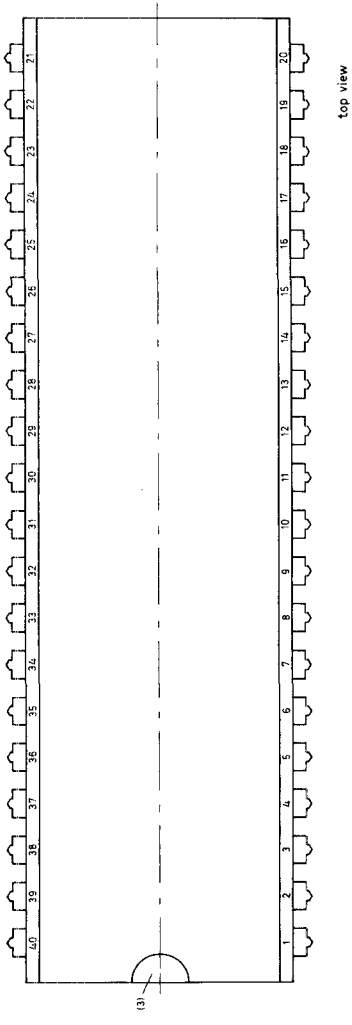
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.

# 40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)




Positional accuracy.

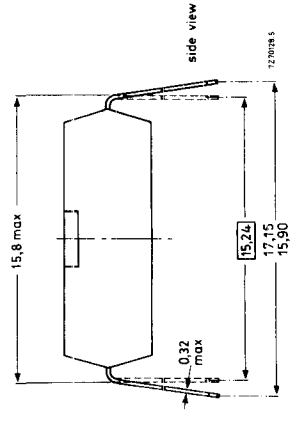
Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

**Dimensions in mm**

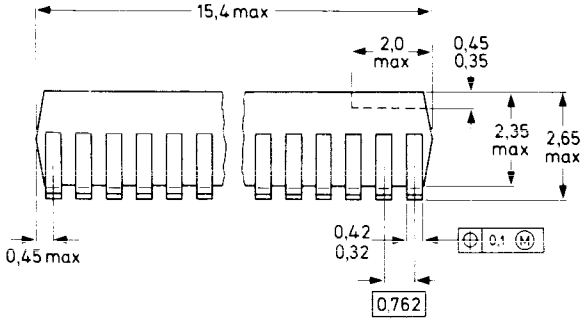


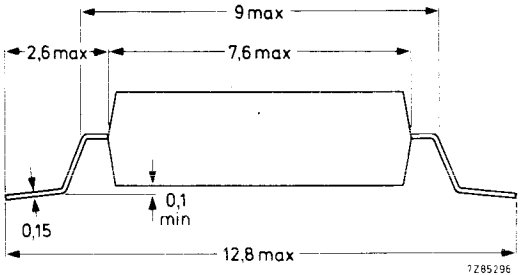

## SOLDERING

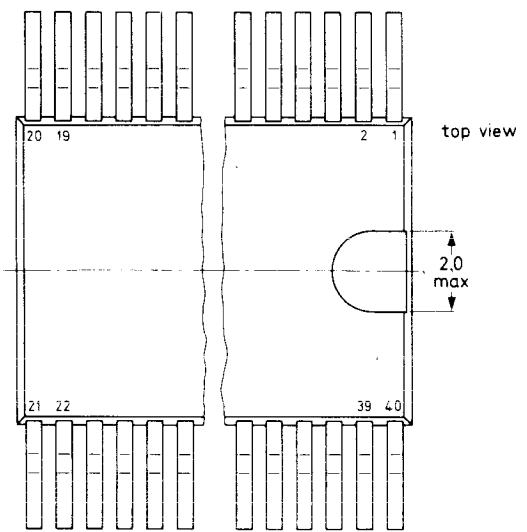
See next page.

Mullard

## 40-LEAD FLAT PACK; PLASTIC (SO-40; SOT-158)




Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

**1. By hand**

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

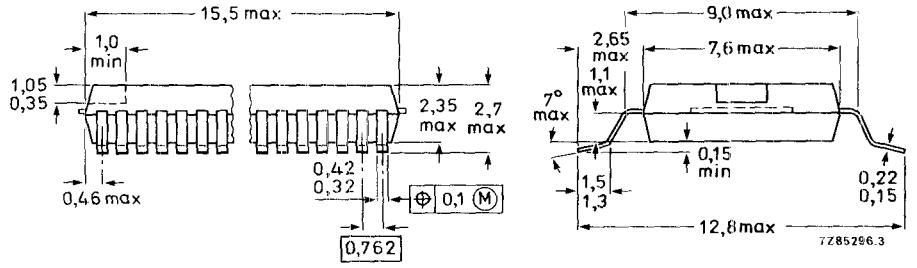
**2. By dip or wave**

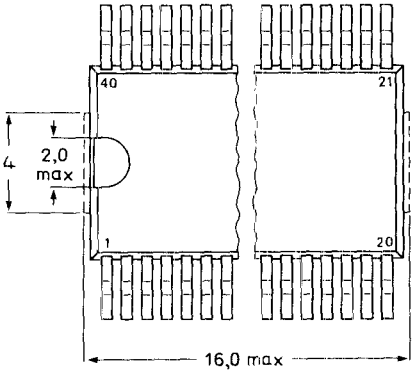
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.

# 40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)




top view

**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

**TEST SOCKET**

Catalogue no.: 7332 150 07601

## SOLDERING

**1. Soldering iron or pulse heated solder tool**

Apply the heating tool to the flat part of the pin only.
Limit the contact time to maximum 10 seconds up to 300 °C, or 5 seconds up to maximum 400 °C.
When using the proper tools, up to 20 pins (at one side of the device) can be soldered in one operation with 2 to 5 seconds and 270 to 320 °C.

**2. By dip or wave**

The maximum permissible temperature of the solder is 260 °C. The permissible total time of immersing the whole package in the bath is 10 seconds, if it is allowed to cool down to less than 150 °C within 6 seconds.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.
If the vertical part of the pin needs heating, reduce the soldering iron temperature to 260 °C.